

Daniel Besse | Digital IC Design Engineer

Swiss – July 9, 1992 • ZH/GR – Switzerland

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Digital IC design engineer with 6 years experience in RFIC applications.

Work Experience

AlpsenTek GmbH

Senior IC Design Engineer, Hybrid Biomimetic Vision Sensors.

SystemVerilog implementation of digital control and readout for pixel array.

Zürich
2021 – current

ACP Advanced Circuit Pursuit AG

Design Engineer, Multi-mode RFIC and SoC devices.

VHDL implementation of signal processing algorithms, SerDes interfaces and wireless communication protocols. Physical RTL-to-GDSII flow using Cadence digital suite. C code for embedded RISC-V core.

Zürich
2016 – 2021

École Polytechnique Fédérale de Lausanne (EPFL)

Internship, 13-bit AD/DA converter design.

Lausanne
4 months, 2014

Texas Instruments

Internship, Automated MCU digital power simulations.

Freising (D)
5 months, 2013

Education

École Polytechnique Fédérale de Lausanne (EPFL)

Bachelor and Master, Electrical Engineering

Master: **Best EE GPA**. Gilbert Hausmann Award. Excellence scholarship. **GPA 5.83/6.00**.

Bachelor: **Best EPFL GPA award** (out of 1800+ students). **GPA 5.91/6.00**.

Lausanne
2010 – 2016

Georgia Institute of Technology

Bachelor, Electrical and Computer Engineering

Senior year as an exchange. **GPA 4.0/4.0**.

Atlanta (USA)
2012 – 2013

Gymnase Auguste Piccard

Swiss Matura, Physics and Application of Maths

Mathematics award. Mention for matura work. Special class for elite sport.

Lausanne
2007 – 2010

Selected Projects

RFIC digital implementation: RTL development for signal processing, control blocks and SerDes interfaces. (ACP)

Full implementation of digital part of RFICs from RTL design, through verification, to EDA physical flow. Specialized entities for wireless 3GPP protocols, signal processing, data and control interfaces (RBDP/DigRFv4/JESD204/SPI/...), processing units, etc. Transition from externally-controlled device in 130 nm to SoC in 28/22 nm.

IP-XACT register banks: IP-XACT descriptions, automation of documentation and implementation. (AlpsenTek)

IP-XACT XML for each IP. Scripts for automated documentation and RTL. SystemVerilog for register banks and APB building blocks. UVM RAL for verification.

Embedded software: SoC firmware and GSM L1 stack for IoT device. (ACP)

C code development for multi-stack SoC with RISC-V core. Real-time stack arbitration and layer 1 for GSM fallback.

Semi-custom digital flow: Extremely high speed digital down converter design. (LSM, EPFL)

Custom-made 28 nm FD-SOI standard cells and digital flow for 50 GS/s polyphase digital down converter design.

Inexact circuits: Circuit and codec level implementation of inexact adder. (ICLAB, EPFL)

Implementation and analysis of different inexact adder architectures, optimizing for audio codec applications.

Languages

Native: French

Fluent: English, German

Basic: Italian

Skills

Experienced: Cadence Digital Tools, VHDL, Tcl, C

Advanced: Verilog, MATLAB, Cadence Virtuoso, PHP

Basic: C++, Perl

Interests

Sport: Triathlon at international level since 2004.

Involvement: Developer and maintainer of several websites, including full training analysis web-app.