Daniel Besse | Digital IC Design Engineer

Swiss – July 9, 1992 • Zürich – Switzerland
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Digital IC design engineer with 5 years experience in RFIC applications.

Work Experience

ACP Advanced Circuit Pursuit AG — Zürich
Design Engineer, Multi-mode RFIC and SoC devices. — *2016 – current*
VHDL implementation of signal processing algorithms, SerDes interfaces and wireless communication protocols.
Physical RTL-to-GDSII flow using Cadence digital suite. C code for embedded RISC-V core.

École Polytechnique Fédérale de Lausanne (EPFL) — Lausanne
Internship, 13-bit AD/DA converter design. — *4 months, 2014*

Texas Instruments — Freising (D)
Internship, Automated MCU digital power simulations. — *5 months, 2013*

Education

École Polytechnique Fédérale de Lausanne (EPFL) — Lausanne
Bachelor and Master, Electrical Engineering — *2010 – 2016*
Master: **Best EE GPA**. Gilbert Hausmann Award. Excellence scholarship. **GPA 5.83/6.00**.
Bachelor: **Best EPFL GPA award** (out of 1800+ students). **GPA 5.91/6.00**.

Georgia Institute of Technology — Atlanta (USA)
Bachelor, Electrical and Computer Engineering — *2012 – 2013*
Senior year as an exchange. **GPA 4.0/4.0**.

Gymnase Auguste Piccard — Lausanne
Swiss Matura, Physics and Application of Maths — *2007 – 2010*
Mathematics award. Mention for matura work. Special class for elite sport.

Selected Projects

RFIC digital implementation: *RTL development for signal processing, control blocks and SerDes interfaces.* (ACP)
Full implementation of digital part of RFICs from RTL design, through simulation- and FPGA-based verification, to EDA physical flow. Specialized entities for wireless 3GPP protocols, signal processing, data and control interfaces (RBDP/DigRFv4/JESD204/SPI/...), processing units, etc. Transition from externally-controlled device in 130 nm to SoC in 28/22 nm.

Embedded software: *SoC firmware and GSM L1 stack for IoT device.* (ACP)
C code development for multi-stack SoC with RISC-V core. Real-time stack arbitration and layer 1 for GSM fallback.

Semi-custom digital flow: *Extremely high speed digital down converter design.* (LSM, EPFL)
Custom-made 28 nm FD-SOI standard cells and digital flow for 50 GS/s polyphase digital down converter design.

Inexact circuits: *Circuit and codec level implementation of inexact adder.* (ICLAB, EPFL)
Implementation and analysis of different inexact adder architectures, optimizing for audio codec applications.

Full-custom 64-bit adder: *Analog implementation of high speed digital circuit.* (LSM, EPFL)
Full-custom Virutoso design of a 64-bit Kogge-Stone dynamic-logic accumulator in 90 nm.

Languages

Native: French
Fluent: English, German
Basic: Italian

Skills

Experienced: Cadence Digital Tools, VHDL, IC Design, Tcl, C, MATLAB
Advanced: Cadence Virtuoso, PHP
Basic: C++, Perl, Verilog, SPICE, Assembly

Interests

Sport: Triathlon at international level since 2004. Current holder of PRO license for Ironman.
Involvement: Developer and maintainer of several websites, including full training analysis web-app.