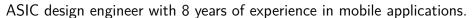
Daniel Besse | Digital IC Design Engineer

Swiss – July 9, 1992 • ZH/GR – Switzerland



I am a dedicated engineer with wide experience in ASIC design and the whole RTL-to-GDSII plus verification flow. In small teams, I have taken responsibility for the design and backend of complex digital systems up to several hundred thousands of gates under the tight deadlines of the mobile industry.



Work Experience

AlpsenTek GmbH

Senior IC Design Engineer, Hybrid biomimetic vision sensors.

Zürich Aug 2021 - current

RTL

SystemVerilog implementation of active pixel sensor (APS) data readout and analog pixel array driving. APB bus structure for configuration register banks and I2C control interface.

IP-XACT

Complete rework of register banks to conform to IP-XACT with auto-generation of SystemVerilog, documentation, C-header files, and UVM register abstraction layer (RAL) database.

Git CI

Deployment of GitLab Continuous Integration pipelines for quality assurance, running lint checks as well as regression test suite. Build management and git repositories setup for digital IP reuse.

ACP Advanced Circuit Pursuit AG

Design Engineer, Multi-mode RFIC and SoC devices.

Mar 2016 - Jul 2021

7ürich

DSP model

MATLAB modeling of transmitter (Rx and Tx) signal processing algorithm. Use of cycle-exact models as golden reference

for hardware design.

RTL

VHDL implementation of digital signal processing (DSP) algorithms, specific modules for 3GPP wireless protocols, as well as SerDes interfaces for data and control (RBDP/DigRFv4/JESD204/SPI/...).

RISC-V SoC

Architecture for system-on-chip in 22 nm including several power domains, a LowRISC ibex core, and legacy signal processing blocks from externally-controlled device in 130 nm.

Physical RTL-to-GDSII flow using Cadence digital suite in both 130 nm and 22 nm.

Backend Firmware

Embedded-C code for multi-stack firmware targetting the internet-of-things (IoT) and running on the RISC-V core of our

own SoC. Real-time stack arbitration and layer 1 for GSM fallback.

Texas Instruments

Freising (D) May - Oct 2013

Intern, Automated MCU digital power simulations for the MSP430.

Power

Firmware testcases and power simulations for MSP430 microcontroller.

Education

École Polytechnique Fédérale de Lausanne (EPFL)

Bachelor and Master, Electrical Engineering

Lausanne 2010-2016

Master

Best EE GPA. Gilbert Hausmann Award. Excellence scholarship. GPA 5.83/6.00.

Master thesis: semi-custom digital flow with custom-made 28 nm FD-SOI standard cells for 50 GS/s digital down converter. Semester project: inexact adder architectures and optimization of the accuracy-resource tradeoff for audio codec applications.

Bachelor

Best EPFL GPA award (out of 1800+ students). GPA 5.91/6.00.

Internship: 13-bit AD/DA converter design using Cadence Virtuoso in a mixed-signal project.



Georgia Institute of Technology

Atlanta (USA) 2012-2013

Bachelor, Electrical and Computer Engineering

Exchange

Senior year (bachelor) as an exchange. GPA 4.0/4.0.

Languages

Skills

Native: French

Experienced: Cadence Digital Tools, VHDL, SystemVerilog, Git, Tcl

Advanced: Bash, Unix, C, MATLAB, Cadence Virtuoso Fluent: English, German Basic: Italian Basic: C++, Perl, Python, Verilog, Microsoft Office



Sport: Triathlon at national and international level for more than 15 years.

Involvement: Developer and maintainer of several websites, including full training analysis web-app using several APIs.