Daniel Besse | Digital IC Design Engineer

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Digital IC design engineer with 5 years experience in RFIC applications.

Work Experience

ACP Advanced Circuit Pursuit AG — **Zürich**
Design Engineer, Multi-mode RFIC and SoC devices. — *2016 – current*
RTL design, verification, and back-end implementation of RFICs targeting smartphones and SoCs for IoT devices. VHDL implementation of signal processing algorithms, specific serial and wireless communication protocols and interfaces. Physical implementation using Cadence digital suite. C-code for ASIC-embedded firmware.

École Polytechnique Fédérale de Lausanne (EPFL) — **Lausanne**
Internship, AD/DA converter design. — *4 months, 2014*
Schematic and layout design of a 13-bit AD/DA converter using Cadence Virtuoso in a mixed-signal project.

Texas Instruments — **Freising (D)**
Internship, Automated Digital Power Simulation — *5 months, 2013*
Development of testcases and automated flows for power simulations of the MSP430 MCUs family.

Education

École Polytechnique Fédérale de Lausanne (EPFL) — **Lausanne**
Master, Electrical Engineering — *2014 – 2016*
Best EE GPA. Gilbert Hausmann Award. Excellence scholarship. **GPA 5.83/6.00**.

Georgia Institute of Technology — **Atlanta (USA)**
Bachelor, Electrical and Computer Engineering — *2012 – 2013*
Senior year as an exchange. **GPA 4.0/4.0**.

École Polytechnique Fédérale de Lausanne (EPFL) — **Lausanne**
Bachelor, Electrical Engineering — *2010 – 2013*
Best EPFL GPA award (out of 1800+ students). **GPA 5.91/6.00**.

Gymnase Auguste Piccard — **Lausanne**
Swiss Matura, Physics and Application of Maths — *2007 – 2010*
Mathematics award. Mention for matura work. Special class for elite sport.

Projects

Master Thesis: *Extremely high speed digital down converter design for wireless communication applications.* (fall 2015)

50 GS/s compressor-based mixer-less polyphase digital down converter design to be integrated with extremely high speed time interleaved ADCs (TI-ADC).

Semester Project: *Circuit and codec level implementation of inexact adder.* (spring 2015)

Implementation and analysis of different inexact adder architectures. Integration and optimization of those adders for audio codec applications.

Advanced VLSI Project: *64-bit Kogge-Stone adder.* (spring 2015)

Full-custom design of a 64-bit Kogge-Stone dynamic-logic accumulator using UMC 90 nm Design Kit in Cadence Virtuoso.

Special Problem: *Temperature Effects on TFET-based Digital Design.* (spring 2013)

TCAD simulation of TFET transistors. Analysis of their use in digital design and of their temperature behavior.

Languages

Mother tongue: French
C1: English, German
B2: Italian

Informatics

Experienced: Cadence Digital Tools, VHDL, Tcl, C, MATLAB
Good: Cadence Virtuoso, C++, PHP
Basic: Verilog, Perl, SPICE, Assembly

Interests

Sport: Triathlon at international level since 2004. Current holder of PRO license for Ironman.

Involvement: Developer and maintainer for different websites, including full training-analysis web-app.